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26. (Amended) A phase-locked loop (PLL) comprising:

an oscillator responsive to a control signal by producing a PLL output signal;

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency, the control circuitry including beat frequency circuitry that detects deviations of the input frequency outside the predetermined input frequency range.

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30. (Amended) A phase-locked loop (PLL) comprising:

an oscillator responsive to a control signal by producing a PLL output signal,

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency, the control circuitry including measurement circuitry which determines whether the PLL input signal's frequency deviates outside the predetermined input frequency range by measuring the voltage of said control signal coupled to the oscillator.

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36. (Amended) An apparatus for providing a synchronized clock signal comprising:

a clock source that produces a clock output signal,

a PLL responsive to the clock output signal, said PLL comprising:

an oscillator responsive to a control signal by producing a PLL output signal;

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a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency, the control circuitry including beat frequency circuitry that detects deviations of the input frequency outside the predetermined input frequency range.

40. (Amended) An apparatus for providing a synchronized clock signal comprising:

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a clock source that produces a clock output signal;

a PLL responsive to the clock output signal, said PLL comprising:

an oscillator responsive to a control signal by producing a PLL output signal;

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency, the control circuitry including measurement circuitry which determines whether the PLL input signal's frequency deviates outside the predetermined input

In view of both the amendments presented above and the following discussion, the Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 and that all of the pending claims satisfy the requirements of 35 U.S.C. § 112. Thus, the applicants believe that all of the claims are now in allowable form.

Objections

A. Claims

Claims 26, 30, 36, 40, and 48 are objected to because of various informalities identified by the Examiner.

In response, the Applicants have amended claims 26, 30, 36, 40, and 48 to correct the identified informalities. In view of these amendments, it is respectfully requested that these objections be withdrawn.

Rejections

A. 35 U.S.C. § 112

The Examiner has rejected claims 27-29 and 37-39 under the provisions of the second paragraph of 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as the invention. In particular, the Examiner alleges that the limitation "the predetermined frequency" in line 1 of claim 27 and line 1 of claim 37, lack antecedent basis.

In response, the Applicants have amended claim 26 to include the term "a predetermined frequency". As claims 27-29 depend either directly or indirectly from claim 26, it is submitted that claims 27-29 now fully conform to 35 U.S.C. § 112.

In addition, the Applicants have amended claim 36 to include the term "a predetermined frequency" in line 12 of claim 36. As claims 37-39 depend either directly or indirectly from claim 36, claims 37-39 now fully conform to 35 U.S.C. § 112.

Having made these changes, the applicants submit that claims 27-29 and 37-39, as they now stand, are definite and hence fully satisfy the requirements of 35 U.S.C. §112.

B. 35 U.S.C. § 102

The Examiner rejected claims 26-29, 36-39, and 49-51 under 35 U.S.C. 102(b) as being anticipated by the Taylor et al. patent (United States patent 5,015,871 issued May 14, 1991, hereinafter "Taylor"). The rejection is respectfully traversed.

Taylor discloses a frequency synthesized, microwave signal generator that uses a microwave harmonic phase locked loop to lock a microwave VCO to a programmable harmonic of a VHF reference crystal oscillator to provide coarse frequency control in steps equal to that reference frequency. (See Taylor, ABSTRACT). The generator further includes means for controlling a frequency synthesizer to generate a fine frequency control signal so as to achieve fine frequency control at the output signal. (See Taylor, Column 2, lines 23-26).

Taylor fails to disclose or suggest at least the invention of claim 26 as follows:

> "A phase-locked loop (PLL) comprising:
>
> an oscillator responsive to a control signal by producing a PLL output signal;
>
> a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the control signal indicative of that difference, the control signal being coupled to the oscillator; and
>
> control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency, the control circuitry including beat frequency circuitry that detects deviations of the input frequency outside the predetermined input frequency range." (emphasis added)

In contrast to the above quoted claim language, Taylor discloses a phase lock loop (PLL) that is responsive to a reference signal from a reference oscillator